REMARKS

Claims 1-5, 7-9, 11-14, and 21-28 are all the claims pending in the application. Claims 15-20 are canceled pursuant to a previous restriction requirement. In addition, claims 6 and 10 are canceled, above, in order to overcome a 35 USC §112, first paragraph, rejection. Further, new claims 21-29 are added to further define the invention. Claims 2, 3, 9, and 13 stand rejected upon informalities. Claims 1-5, 7-9, and 11-14 stand rejected on prior art grounds. In addition, the drawings and specification are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. Rule 83 Objections to Drawings

The drawings stand objected to upon various grounds. First, the drawings are objected to as not showing the features defined by claims 6 and 13. Claims 6 and 13 have been canceled in order to overcome this objection.

Next, the Office Action states that number "21" illustrates different layers in Figures 2E and 2F. In response thereto, Applicants note that paragraph 45 explains that the epitaxially grown semiconductor layer 21 is optionally formed over the substrates 16, 26, as shown in Figure 2E. Paragraph 47 explains that the semiconductor devices 30, 32 are then formed over the semiconductor layer 21 in Figure 2F. Thus, the only difference between Figure 2E and Figure 2F is the addition of the semiconductor devices 30, 32 and drawings are otherwise consistent. Therefore, layer 21 is used consistently between Figures 2E and 2F and is not intended to refer to different layers. Applicants submit that layer 21 represents the same layer in both Figures 2E and 2F, and that such description is consistent with the specification.

Applicants note that it is not clear whether the objection relates to the difference in the thickness of layer 21 between Figures 2E and 2F. Applicants first note that patent drawings are schematic drawings and therefore not necessarily drawn to scale and that some slight difference in the thicknesses of the same layer can vary from drawing to drawings, especially in informal

hand drawings. Further, Applicants submit herewith a substitute informal drawing sheet which increases the thickness of the layer 21 in Figure 2E. Further, formal drawings are in the process of being prepared and the formal drawings will show a more consistent thickness of layer 21 between Figures 2E and 2F.

The Office Action also states that there are inconsistencies regarding layers 21, 23, and 30 in Figures 2E-2G. Applicants first note that Figure 2G illustrates a different embodiment than the embodiment shown in Figures 2E and 2F. As explained in paragraph 48, in the embodiment shown in Figure 2G, the straining layer 23 is formed after the gate conductors 30, 32 and sources and drains of the transistors are formed. To the contrary, in Figures 2E and 2F, the semiconductor layer 21 is formed before the devices 30, 32 are formed (paragraph 45). Further, the semiconductor layer 21 is an optional layer and therefore does not need to be included in the structure shown in Figure 2G. Therefore, the inconsistencies regarding layers 21 and 23 are intended to be so because different embodiments are being described and because layer 21 is an optional layer.

In view of the foregoing, Applicants submit that layers 21, 23 and structures 30 are properly illustrated in the drawings as described by the specification. Therefore, the Examiner is respectfully requested to reconsider and withdrawn this objection.

II. The Objection to the Specification

In response to the objection to the Specification, the Specification has been amended as suggested in the Office Action. More specifically, in paragraph 54, the term "21" has been changed to "23". In view of the foregoing, the Examiner is respectfully requested to reconsider and withdrawn this objection.

III. The Objections to the Claims

The Office Action objects to claims 3 and 10 as failing to clearly identify the transistor

with which the claimed gate is associated. In response, claims 3 and 10 have been amended to define that each of the transistors includes source and drain regions and a gate. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this objection.

IV. The 35 U.S.C. §112, First Paragraph, Rejection

Claims 2, 3, 9, and 13 stand rejected under 35 U.S.C. §112, first paragraph. More specifically, the Office Action states that it is not clear how the straining layer can be used in combination with the silicide layer and that the material makeup of the straining layer is not provided. The Office Action argues that it is not clear how the straining layer can have the desired straining effect on the underlying transistors if the straining layer is separated from the substrate by the silicide layer, especially because the silicide layer is normally formed through and annealing process which would tend to relax the underlying source and drain regions.

First, Applicants note materials used for straining layers are very well-known and that the specific material utilized to create straining in an adjacent layer depends on the material makeup of the adjacent layer and that one ordinarily skilled in the art would understand that many different types of materials can be utilized to create strain. For example, even some of the applied prior art references (Ge et al. and Wang et al.) discloses some of the common materials utilize as a straining layer (see paragraph 29 of Ge et al.). Therefore, Applicants submit that one ordinarily skilled in the art would be able to make and use the claimed invention because the material makeup and utilization of straining layers is described extensively in conventional teachings.

With respect to the intervening silicide layer between the straining layer and the underlying conductor and source/drain, Applicants agree that if the annealing process for the silicide was performed after the straining layer was formed, there may be some relaxation of the straining; however, because of the silicide is formed (and any associated annealing processes are performed) before the straining layer is formed, the silicide does not affect the strain produced by the straining layer. It is well-known that a silicide layer formed on a material will have

approximately the same coefficient of thermal expansion as the underlying material because the material properties of the silicide layer are strongly based upon the underlying material from which the silicide layer is formed. Therefore, the straining layer will still produced strain within the silicide layer and underlying material because both have similar coefficients of thermal expansion, which are different from that of the straining layer, which induces the straining the first place. Therefore, because the invention forms the straining layer after the silicide layer is formed (forms the straining layer on the silicide layer) the straining layer is equally as effective as if it had been formed directly upon the underlying material (the conductor, source/drain).

In addition, Applicants note that the limitation regarding one type of transistor being strained and another type of transistor not being strained has been removed from the claims, thereby rendering the rejection of claims 6 and 10 moot. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo et al., hereinafter Yeo in view of Ge et al., hereinafter "Ge", and/or Wang et al., hereinafter "Wang". Applicants respectfully traverse this rejections because the references do not teach or suggest the inventive structure illustrated, for example, in Figure 2G were one portion of the substrate includes a layer having a first crystalline orientation 16 and a layer having a second crystalline orientation 12, with the other portion of the substrate including a layer having the second crystalline orientation 12, 26 and which is devoid of the layer having the first crystalline orientation 12. Ge and Wang are utilized merely to demonstrate a teaching of straining layers and only Yeo is relied upon for teaching regions having different crystalline orientations. Yeo discloses that the transistors can be formed on islands that have different crystalline orientations 110, 112, but Yeo does not teach or suggest a structure were one portion of the substrate includes a layer having a first crystalline orientation and a layer having a second crystalline orientation, with the other portion of the substrate including a layer having the second crystalline orientation

and which is devoid of the layer having the first crystalline orientation. Therefore, it is Applicants position that the prior art of record does not teach or suggest the claimed invention.

More specifically, independent claim defines that the "first portions of said substrate comprise a layer having said first type of crystalline orientation and a layer having said second type of crystalline orientation, and wherein said second portions of said substrate comprise said layer having said second type of crystalline orientation and are devoid of said layer having said first type of crystalline orientation." Independent claim 8 a similarly defines that "one of said first portions and said second portions of said substrate comprise a layer having said first type of crystalline orientation and a layer having said second type of crystalline orientation, and wherein the other of said first portions and said second portions of said substrate comprise a layer having one of said first type of crystalline orientation and said second type of crystalline orientation and are devoid of a layer having the other of said first type of crystalline orientation and said second type of crystalline orientation." Applicants submit that the structures defined by independent claims 1 and 8 are fully disclosed in specification and illustrated in the drawings. For example, as shown in Figure 2G, one portion of the substrate includes a layer having a first crystalline orientation 16 and a layer having a second crystalline orientation 12, with the other portion of the substrate including a layer having the second crystalline orientation 12, 26 and which is devoid of the layer having the first crystalline orientation 12. The structure is available because, as shown in Figure 2A, the invention begins with a laminated substrate that is eventually etched (Figure 2C) down to the layer of second crystalline orientation 12 to allow additional material 26 of the second crystalline orientation to be formed (Figure 2D). The resulting structure shown in Figure 2G, includes one portion of the substrate having a first crystalline orientation layer 16 and a layer having a second crystalline orientation 12, with the other portion of the substrate including a layer having the second crystalline orientation 12, 26 and which is devoid of the layer having the first crystalline orientation 12.

To the contrary, Yeo forms islands on the substrate that have different crystalline orientations. All of the structures that utilize different crystalline orientation within Yeo are built on top of the substrate and do not comprise layers within the substrate as in the claimed

invention. Therefore, the structure according to Yeo requires substantially more complicated and expensive processing than the claimed invention which begins with the laminated structure shown in Applicants Figure 2A. Therefore, the inventive structure is superior when compared to the structure disclosed in Yeo (whether combined with Ge and/or Wang or not) because the inventive structure can be produced with a substantially simplified, less expensive, and higher yielding manufacturing process. Further, the claimed structure produces a number of other advantages, such as reduced height, reduced weight and size, reduced amount of materials, etc. when compared to the silicon island structures disclosed in Yeo.

Therefore, as shown above, it is Applicants position that the prior art of record does not teach or suggest a structure where the "first portions of said substrate comprise a layer having said first type of crystalline orientation and a layer having said second type of crystalline orientation, and wherein said second portions of said substrate comprise said layer having said second type of crystalline orientation and are devoid of said layer having said first type of crystalline orientation" as defined by independent claim 1, or a structure where "one of said first portions and said second portions of said substrate comprise a layer having said first type of crystalline orientation and a layer having said second type of crystalline orientation, and wherein the other of said first portions and said second portions of said substrate comprise a layer having one of said first type of crystalline orientation and said second type of crystalline orientation and are devoid of a layer having the other of said first type of crystalline orientation and said second type of crystalline orientation" as defined by independent claim 8. Thus, it is Applicants position that independent claims 1 and 8 are patentable over the prior art of record. Further, independent claims 2-5, 7, 9, and 11-14 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. Conclusion

In view of the foregoing, Applicants submit that claims 1-5, 7-9, 11-14, and 21-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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